

6/18/04

PTO/SB/08a (08-03)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Application Number	TBD
				Filing Date	Herewith 04/13/04
				First Named Inventor	Yang, et al.
				Art Unit	TBD 2814
				Examiner Name	TBD T. DOAN
Sheet	1	of	1	Attorney Docket Number	TSM03-0929

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
TD		US-6,222,234 B1	04-24-2001	Imai	
TD		US-6,413,802 B1	07-02-2002	Hu et al.	
		US-			
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FOREIGN PATENT DOCUMENTS						
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TD		CHAU, R., et al., "A 50nm Depleted-Substrate CMOS Transistor (DST)," IEDM (2001) pp. 621-624.	
TD		SHAHIDI, G.G., "SOI Technology for the GHz Era," IBM J. RES. & DEV., Vol. 46, No. 2/3 (March/May 2002) pp. 121-131.	

Examiner Signature	<i>T. Doan</i>	Date Considered	12/05/03
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